VLSI

BV001VLSI14 DESIGN FLOW FOR FLIP-FLOP GROUPING IN DATA-DRIVEN CLOCK GATING (IEEE APR 2014)

BV002VLSI13 NEW HIGH-SPEED MULTIOUTPUT CARRY LOOK-AHEAD ADDERS (IEEE SEP 2013)

BV003VLSI14 A FULLY STATIC TOPOLOGICALLY-COMPRESSED 21-TRANSISTOR FLIP-FLOP WITH 75% POWER SAVING (IEEE NOV 2014)

BV004VLSI15 HIGH-SPEED AND ENERGY-EFFICIENT CARRY SKIP ADDER OPERATING UNDER A WIDE RANGE OF SUPPLY VOLTAGE LEVELS (IEEE MAR 2015)

BV005VLSI15 DESIGN OF A LOW POWER 4X4 MULTIPLIER BASED ON FIVE TRANSISTOR (5-T) HALF ADDER, EIGHT TRANSISTOR (8-T) FULL ADDER & TWO TRANSISTOR (2-T) AND GATE (IEEE FEB 2015)

BV006VLSI15 ENERGY AND AREA EFFICIENT THREE-INPUT XOR/XNORS WITH SYSTEMATIC CELL DESIGN METHODOLOGY (IEEE MAR 2015)

BV007VLSI14 DEVELOPMENT OF AN FPGA-BASED SPWM GENERATOR FOR HIGH SWITCHING FREQUENCY DC/AC INVERTERS (IEEE JAN 2014)

BV008VLSI15 NOVEL FPGA IMPLEMENTATION OF HAND SIGN RECOGNITION SYSTEM WITH SOM-HEBB CLASSIFIER (IEEE 2015)

BV009VLSI14 DESIGN OF LOW POWER AND HIGH SPEED MODIFIED CARRY SELECT ADDER FOR 16 BIT VEDIC MULTIPLIER

BV010VLSI15 ENERGY-EFFICIENT APPROXIMATE MULTIPLICATION FOR DIGITAL SIGNAL PROCESSING AND CLASSIFICATION APPLICATIONS (IEEE JUL 2014)

BV011VLSI14 AREA-DELAY-POWER EFFICIENT CARRY-SELECT ADDER (IEEE JUNE 2014)

BV012VLSI14 FAULT TOLERANT PARALLEL FILTERS BASED ON ERROR CORRECTION CODES (IEEE MAR 2014)

BV013VLSI14 SINGLE-ERROR-CORRECTION AND DOUBLE-ADJACENT-ERROR-CORRECTION CODE FOR SIMULTANEOUS TESTING OF DATA BIT AND CHECK BIT ARRAYS IN MEMORIES (IEEE MAR 2014)

BV014VLSI08 FUNCTIONAL DESIGN OF FPGA IN A BRUSHLESS DC MOTOR SYSTEM BASED ON FPGA AND DSP

BV015VLSI12 STABILITY ANALYSIS OF FPGA-BASED CONTROL OF BRUSHLESS DC MOTORS AND GENERATORS USING DIGITAL PWM TECHNIQUE

BV016VLSI13 FPGA BASED SPEED CONTROL OF BRUSHLESS DC MOTORS USING IOPT PETRI NET MODELS
BV018VLSI13 EFFICIENT METHOD FOR CONTROLLING ELECTRIC POWER BY AUTOMATED MONITORING SYSTEM USING FPGA

BV019VLSI13 IMPLEMENTATION OF FPGA BASED CONTROLLER FOR INDUCTION MOTOR DRIVES

BV020VLSI15 FAULT TOLERANT PARALLEL FFTS USING ERROR CORRECTION CODES AND PARSEVAL CHECKS

BV021VLSI12 DESIGN OF LOW POWER ALU USING 8T FA AND PTL BASED MUX CIRCUITS

BV022VLSI12 SDMLP: ON THE USE OF COMPLEMENTARY PASS TRANSISTOR LOGIC FOR DESIGN OF DPA RESISTANT CIRCUITS

BV023VLSI12 NOVEL ULTRA LOW-VOLTAGE AND HIGH-SPEED CMOS PASS TRANSISTOR LOGIC

BV024VLSI12 ENERGY-DELAY EFFICIENT ASYNCHRONOUS-LOGIC 16×16-BIT PIPELINED MULTIPLIER BASED ON SENSE AMPLIFIER-BASED PASS TRANSISTOR LOGIC

BV025VLSI13 DESIGN AND SIMULATION OF HYBRID SET-MOS PASS TRANSISTOR LOGIC BASED UNIVERSAL LOGIC GATES

BV026VLSI13 DIFFERENTIAL HIGH SPEED ULTRA LOW-VOLTAGE PASS TRANSISTOR BOOLEAN LOGIC

BV027VLSI14 IMPLEMENTATION OF AREA AND ENERGY EFFICIENT FULL ADDER CELL

BV028VLSI10 A 10-BIT LOW-POWER SMALL-AREA HIGH-SWING CMOS DAC

BV029VLSI14 LOW-POWER PULSE-TRIGGERED FLIP-FLOP DESIGN BASED ON A SIGNAL FEED-THROUGH SCHEME

BV030VLSI13 DESIGN OF LOW POWER SEQUENTIAL CIRCUIT USING CLOCKED PAIR SHARED FLIP FLOP

BV031VLSI13 CLOCK GATING BASED ENERGY EFFICIENT ALU DESIGN AND IMPLEMENTATION ON FPGA

BV032VLSI13 DESIGN OF A LOW-POWER PULSE-TRIGGERED FLIP-FLOP WITH CONDITIONAL CLOCK TECHNIQUE

BV033VLSI13 REAL TIME FPGA IMPLEMENTATION OF BRUSHLESS DC MOTOR CONTROL USING SINGLE CURRENT SENSOR

BV034VLSI13 HIGH PERFORMANCE LOW POWER DUAL EDGE TRIGGERED STATIC D FLIP-FLOP

BV035VLSI13 DESIGN OF LOW POWER PULSED FLIP-FLOP USING SLEEP TRANSISTOR SCHEME
A NEW STRUCTURE OF LOW-POWER AND LOW-VOLTAGE DOUBLE-EDGE TRIGGERED FLIP-FLOP

DESIGN OF SEQUENTIAL CIRCUITS IN MULTILAYER QCA STRUCTURE

DESIGN AND ANALYSIS OF A SIMPLE D FLIP-FLOP BASED SEQUENTIAL LOGIC CIRCUITS FOR QCA IMPLEMENTATION

LOW STATIC AND DYNAMIC POWER MTCMOS BASED 12T SRAM CELL FOR HIGH SPEED MEMORY SYSTEM

LEAKAGE POWER REDUCTION IN DATA DRIVEN DYNAMIC LOGIC CIRCUITS

QCA BASED SEQUENTIAL AND COMBINATIONAL CIRCUIT DESIGN AND IMPORTANCE OF PARASITIC COMPONENTS

LOW POWER DUAL EDGE TRIGGERED FLIP-FLOP

DESIGN OF A 4-BIT ADDER USING REVERSIBLE LOGIC IN QUANTUM-DOT CELLULAR AUTOMATA (QCA)

A 24-TRANSISTOR STATIC FLIP-FLOP CONSISTING OF NORS AND INVERTERS FOR LOW-POWER DIGITAL VLSIS

A NOVEL RATIOED LOGIC STYLE FOR FASTER SUBTHRESHOLD DIGITAL CIRCUITS BASED ON 90 NM CMOS AND BELOW

EFFICIENT REALIZATION OF DIGITAL LOGIC CIRCUIT USING QCA MULTIPLEXER

ONE-BIT NON-VOLATILE MEMORY CELL USING MEMRISTOR AND TRANSMISSION GATES

A LOW POWER CMOS FLIP-FLOP FOR HIGH PERFORMANCE PROCESSORS

AN IMPLEMENTATION OF 1- BIT LOW POWER FULL ADDER BASED ON MULTIPLEXER AND PASS TRANSISTOR LOGIC

LOW-POWER COMPARATOR DESIGN BASED ON CMOS DYNAMIC LOGIC CIRCUIT

POWER ANALYSIS AND COMPARISON OF CLOCK GATED TECHNIQUES IMPLEMENTED ON A 16-BIT ALU

SELF DRIVEN PASS-TRANSISTOR BASED LOW-POWER PULSE TRIGGERED FLIP-FLOP DESIGN

LOW-POWER CLOCK DISTRIBUTION USING A CURRENT-PULSED CLOCKED FLIP-FLOP

IMPLEMENTATION OF LOW POWER FLIP FLOP DESIGN IN NANOMETER REGIME
**BV055VLSI15** IMPLEMENTATION OF HIGH PERFORMANCE SRAM CELL USING TRANSMISSION GATE

**BV056VLSI15** AN EFFICIENT DESIGN TECHNIQUE FOR LOW POWER DYNAMIC FEEDTHROUGH LOGIC WITH ENHANCED PERFORMANCE FOR WIDE FAN-IN GATES

**BV057VLSI15** DYNAMIC THRESHOLD SOURCE COUPLED LOGIC WITH PUSHPULL TOPOLOGY FOR ULTRA LOW POWER APPLICATIONS

**BV058VLSI15** DESIGN OF NOVEL INVERTER AND BUFFER IN QUANTUM-DOT CELLULAR AUTOMATA (QCA)

**BV059VLSI15** DESIGN AND ANALYSIS OF ODD- AND EVEN-PARITY GENERATORS AND CHECKERS USING QUANTUM-DOT CELLULAR AUTOMATA (QCA)

**BV060VLSI15** LOW POWER FLIP FLOP MERGING TECHNIQUE BY CRITICAL PATH DELAY ANALYSIS

**WIRELESS**

**BV001WL13** WIRELESS SENSOR NETWORK FOR MULTI-STOREY BUILDING: DESIGN AND IMPLEMENTATION (IEEE JAN 2013)

**BV002WL13** MANAGEMENT OF MECHANICAL VIBRATION AND TEMPERATURE IN SMALL WIND TURBINES USING ZIGBEE WL NETWORK (IEEE FEB 2013)

**BV003WL14** SENSORLESS ILLUMINATION CONTROL OF A NETWORKED LED-LIGHTING SYSTEM USING FEEDFORWARD NEURAL NETWORK (IEEE APR 2014)

**BV004WL14** AUTOMATED IRRIGATION SYSTEM USING A WIRELESS SENSOR NETWORK AND GPRS MODULE (IEEE 2014)

**BV005WL14** ROBUST CONTROL FOR URBAN ROAD TRAFFIC NETWORKS (IEEE FEB 2014)

**BV006WL14** AN INTEGRATED SYSTEM FOR REGIONAL ENVIRONMENTAL MONITORING AND MANAGEMENT BASED ON INTERNET OF THINGS (IEEE 2014)

**BV007WL14** A RECONFIGURABLE SMART SENSOR INTERFACE FOR INDUSTRIAL WSN IN IOT ENVIRONMENT (IEEE MAY 2014)

**BV008WL14** EARLIEST-DEADLINE-BASED SCHEDULING TO REDUCE URBAN TRAFFIC CONGESTION

PRACTICAL SECURE COMMUNICATION FOR INTEGRATING WL SENSOR NETWORKS INTO THE INTERNET OF THINGS (IEEE OCT 2013)

ACCESSIBLE DISPLAY DESIGN TO CONTROL HOME AREA NETWORKS (IEEE MAY 2013)
DYNAMIC ULTRASONIC HYBRID LOCALIZATION SYSTEM FOR INDOOR MOBILE ROBOTS (IEEE OCT 2013)
LOW POWER WL SENSOR NETWORK FOR BUILDING MONITORING (IEEE MARCH 2013)
IN-BUILDING LIGHTING MANAGEMENT SYSTEM WITH WL COMMUNICATIONS (IEEE 2012)

**Artificial intelligence**

**BV001NURL** ARTIFICIAL NEURAL NETWORK AND PID BASED CONTROL SYSTEM FOR DC MOTOR DRIVES

**BV002NURL13** NEURAL NETWORK BASED CLASSIFICATION OF POLLEN GRAINS

**BV003NURL14** ADAPTIVE NEURAL NETWORK CONTROL OF ROBOT BASED ON A UNIFIED OBJECTIVE BOUND

**BV004NURL13** MULTIRESOLUTION TECHNIQUE TO HANDWRITTEN ENGLISH CHARACTER RECOGNITION USING LEARNING RULE AND EUCLIDEAN DISTANCE METRIC

**BV005NURL14** REVIEW OF HANDWRITTEN PATTERN RECOGNITION OF DIGITS AND SPECIAL CHARACTERS USING FEED FORWARD NEURAL NETWORK AND IZHIKEVICH NEURAL MODEL

**BV006NURL14** DISTRIBUTED DETECTION IN NEURAL NETWORK BASED MULTIHOP WIRELESS SENSOR NETWORK

**BV007NURL** ESTIMATION OF SOIL MOISTURE PROFILE USING WAVELET NEURAL NETWORKS

**BV008NURL14** RECOGNITION OF A HUMAN BEHAVIOR PATTERN IN PAPER ROCK SCISSOR GAME USING BACKPROPAGATION ARTIFICIAL NEURAL NETWORK METHOD

**BV009NURL14** ROBOT CONTROL USING HIGH DIMENSIONAL NEURAL NETWORKS

**BV010NURL14** IMAGE CHARACTER RECOGNITION USING DEEP CONVOLUTIONAL NEURAL NETWORK LEARNED FROM DIFFERENT LANGUAGES

**BV011NURL14** OFFLINE HANDWRITTEN WRITER INDEPENDENT TAMIL CHARACTER RECOGNITION

**BV012NURL14** KHMER CHARACTER RECOGNITION USING ARTIFICIAL NEURAL NETWORK NEURAL NETWORK BASED IMAGE PROCESSING

REGION BASED TRAFFIC LIGHT CONTROLLER (IEEE 2004)

CHARACTER RECOGNITION USING FEED FORWARD NEURAL NETWORK

LICENSE PLATE RECOGNITION SYSTEM (IEEE)

NEURAL NETWORK BASED TRACK ASSISTANCE SYSTEM FOR TRAINS
NEURAL NETWORK AUTO SIGNALING SYSTEM FOR TRAINS
NEURAL NETWORK BASED SERVO POSITIONING SYSTEM
NEURAL NETWORK BASED DC MOTOR SPEED CONTROLLER
NEURAL BASED TARGET SENSING SYSTEM
NEURAL BASED SIGNATURE VERIFICATION SYSTEM

Image processing
RECONSTRUCTION-BASED METRIC LEARNING FOR UNCONSTRAINED FACE VERIFICATION.
AN INNOVATIVE LOSSLESS COMPRESSION METHOD FOR DISCRETE-COLOR IMAGES
LATENT FINGERPRINT ENHANCEMENT VIA MULTI-SCALE PATCH BASED SPARSE REPRESENTATION
EFFICIENT VESSEL FEATURE DETECTION FOR ENDOSCOPIC IMAGE ANALYSIS
MULTIMODAL NEUROIMAGING FEATURE LEARNING FOR MULTICLASS DIAGNOSIS OF ALZHEIMERS DISEASE
AN AUTOMATIC FACE DETECTION AND GENDER CLASSIFICATION FROM COLOR IMAGES USING SUPPORT VECTOR MACHINE
3-D WARPED DISCRETE COSINE TRANSFORM FOR MRI IMAGE COMPRESSION
RECURSIVE HISTOGRAM MODIFICATION: ESTABLISHING EQUIVALENCY BETWEEN REVERSIBLE DATA HIDING AND LOSSLESS DATA COMPRESSION
AUTOMATIC LICENSE PLATE RECOGNITION (ALPR): A STATE-OF-THE-ART REVIEW
WHAT ARE WE TRACKING: A UNIFIED APPROACH OF TRACKING AND RECOGNITION
HUMAN IDENTIFICATION USING PALM-VEIN IMAGES
FINGERPRINT COMBINATION FOR PRIVACY PROTECTION

EMBEDDED
BV001EMBD13 PRECISE MOISTURE MONITORING FOR VARIOUS SOIL TYPES USING HANDHELD MICROWAVE-SENSOR METER
BV002EMBD13 DEHEMS: CREATING A DIGITAL ENVIRONMENT FOR LARGE-SCALE ENERGY MANAGEMENT AT HOMES
BV003EMBD14 ROBUST CONTROL FOR URBAN ROAD TRAFFIC NETWORKS
**DESIGN OF INTELLIGENT TRAFFIC LIGHT CONTROLLER USING EMBEDDED SYSTEM**

**EARLIEST-DEADLINE-BASED SCHEDULING TO REDUCE URBAN TRAFFIC CONGESTION**

**LIMITED PREEMPTIVE SCHEDULING FOR REAL-TIME SYSTEMS. A SURVEY**

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